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PTO/SB/05 (08-00)

**UTILITY  
PATENT APPLICATION  
TRANSMITTAL**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	I-2-116.1US
First Inventor	Kaewell, Jr. et al.
Title	CODE DIVISION MULTIPLE ACCESS MODEM INTERFACE
Express Mail Label No.	EL649759521US

**APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)  
(Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status.  
See 37 CFR 1.27.
3. ☒ Specification [Total Pages  ]  
(preferred arrangement set forth below)
  - Descriptive title of the invention
  - Cross Reference to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to sequence listing, a table, or a computer program listing appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claim(s)
  - Abstract of the Disclosure
4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets  ]
5. Oath or Declaration [Total Pages  ]
  - a. ☐ Newly executed (original or copy)  
Copy from a prior application (37 CFR 1.63 (d))
  - b. ☐ (for continuation/divisional with Box 17 completed)
  - i. ☐ **DELETION OF INVENTOR(S)**  
Signed statement attached deleting inventor(s)  
named in the prior application, see 37 CFR  
1.63(d)(2) and 1.33(b)
6. ☐ Application Data Sheet. See 37 CFR 1.76

**ADDRESS TO:**Commissioner for Patents  
Box Patent Application  
Washington, DC 20231

7. ☐ CD-ROM or CD-R in duplicate, large table or  
Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission  
(if applicable, all necessary)
  - a. ☐ Computer Readable Form (CRF)
  - b. Specification Sequence Listing on:
    - i. ☐ CD-ROM or CD-R (2 copies); or
    - ii. ☐ paper
  - c. ☐ Statements verifying identity of above copies

**ACCOMPANYING APPLICATION PARTS**

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 CFR 3.73(b) Statement ☐ Power of  
(when there is an assignee) Attorney
11. ☐ English Translation Document (if applicable)
12. ☐ Information Disclosure ☐ Copies of IDS  
Statement (IDS)/PTO-1449 Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)  
(Should be specifically itemized)
15. ☐ Certified Copy of Priority Document(s)  
(if foreign priority is claimed)
16. ☒ Other: Communication Under Rule 37 C.F.R.  
§1.53(b)

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP)

of prior application No. \_\_\_\_\_ / \_\_\_\_\_

Prior application information:

Examiner \_\_\_\_\_

Group / Art Unit: \_\_\_\_\_

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

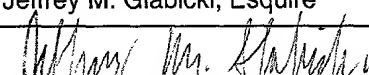
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Signature			Date 10/27/00

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**FEE TRANSMITTAL  
for FY 2000**

Patent fees are subject to annual revision.

**TOTAL AMOUNT OF PAYMENT** (\$ 844.00)**Complete if Known**

Application Number	Not Yet Known
Filing Date	Not Yet Known
First Named Inventor	Kaewell, Jr. et al.
Examiner Name	Not Yet Known
Group Art Unit	Not Yet Known
Attorney Docket No.	I-2-116.1US

**METHOD OF PAYMENT (check one)**

- 1.
- ☒
- The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

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Deposit Account Name **InterDigital Comm. Corp.**

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17☐ Applicant claims small entity status. See 37 CFR 1.27

- 2.
- ☐
- Payment Enclosed:**

☐ Check ☐ Credit card ☐ Money Order ☐ Other**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
101 710	201 355	Utility filing fee	710
106 320	206 160	Design filing fee	
107 490	207 245	Plant filing fee	
108 710	208 355	Reissue filing fee	
114 150	214 75	Provisional filing fee	

**SUBTOTAL (1)** (\$ 710.00)**2. EXTRA CLAIM FEES**

Total Claims	Extra Claims	Fee from below	Fee Paid
23	-20** = 3	18	54
4	-3** = 1	80	80
			0

\*\*or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
103 18	203 9	Claims in excess of 20
102 80	202 40	Independent claims in excess of 3
104 270	204 135	Multiple dependent claim, if not paid
109 80	209 40	** Reissue independent claims over original patent
110 18	210 9	** Reissue claims in excess of 20 and over original patent

**SUBTOTAL (2)** (\$ 134.00)**FEE CALCULATION (continued)****3. ADDITIONAL FEES**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105 130	205 65	Surcharge - late filing fee or oath	
127 50	227 25	Surcharge - late provisional filing fee or cover sheet	
139 130	139 130	Non-English specification	
147 2,520	147 2,520	For filing a request for <i>ex parte</i> reexamination	
112 920*	112 920*	Requesting publication of SIR prior to Examiner action	
113 1,840*	113 1,840*	Requesting publication of SIR after Examiner action	
115 110	215 55	Extension for reply within first month	
116 390	216 195	Extension for reply within second month	
117 890	217 445	Extension for reply within third month	
118 1,390	218 695	Extension for reply within fourth month	
128 1,890	228 945	Extension for reply within fifth month	
119 310	219 155	Notice of Appeal	
120 310	220 155	Filing a brief in support of an appeal	
121 270	221 135	Request for oral hearing	
138 1,510	138 1,510	Petition to institute a public use proceeding	
140 110	240 55	Petition to revive - unavoidable	
141 1,240	241 620	Petition to revive - unintentional	
142 1,240	242 620	Utility issue fee (or reissue)	
143 440	243 220	Design issue fee	
144 600	244 300	Plant issue fee	
122 130	122 130	Petitions to the Commissioner	
123 50	123 50	Petitions related to provisional applications	
126 240	126 240	Submission of Information Disclosure Stmt	
581 40	581 40	Recording each patent assignment per property (times number of properties)	
146 710	246 355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149 710	249 355	For each additional invention to be examined (37 CFR § 1.129(b))	
179 710	279 355	Request for Continued Examination (RCE)	
169 900	169 900	Request for expedited examination of a design application	

Other fee (specify) \_\_\_\_\_

\* Reduced by Basic Filing Fee Paid

**SUBTOTAL (3)** (\$ 0.00)**SUBMITTED BY**

Name (Print/Type) **Jeffrey M. Glabicki, Esquire**

Signature *Jeffrey M. Glabicki*

Registration No. (Attorney/Agent) **42,584****Complete (if applicable)**

Telephone **215-568-6400**

Date **10/27/00**

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## CODE DIVISION MULTIPLE ACCESS MODEM INTERFACE

This application claims priority from U.S. Provisional Application No. 60/192,230, filed on March 27, 2000.

### BACKGROUND

5       The present invention generally relates to wireless communication networks. In particular, the invention relates to modem interfaces used in wireless communication networks.

10       Modem interfaces as used in wireless communication networks, such as code division multiple access (CDMA) wireless networks, are commonly used to transfer data between wired components of the network and a wireless air interface 38 of the network. Figure 1 illustrates a simplified wireless communication network. A user terminal 20 is connected to a local exchange 22. The user terminal 20 transmits data over the local exchange 22 through a radio distribution unit (RDU) 24.

15       The data sent through the RDU 24 is received by a modem 28 in a radio carrier station (RCS) 26 prior to transmission over the air interface 38. The modem interface 34 takes the data that was transferred over the local exchange 22 and RDU 24 and converts it into a format compatible with the transmit circuitry 36 of the modem 28. The transmit circuitry 36 converts the data into a format suitable for transmission over the wireless air interface 38. The data is subsequently transmitted over the air interface 38 by the base  
20       station 30 and received by an antenna 42 at a radio network terminal (RNT) 40. The received signals are processed by the receive circuitry 32 of the RNT's modem 28. The processed signals are sent to a modem interface 34 which converts the signals into a format

I-2-116.1US

to be sent to a second user terminal 46.

Conversely, data to be sent by the second user terminal 46 is sent to the modem interface 34 of the RNT 40. The data is processed to be in a format suitable for the transmit circuitry 32 of the modem 28. The transmit circuitry 36 converts the processed data into a format suitable for transfer over the air interface 38. The data is subsequently transmitted over the air interface 38 using an antenna 42 and received by the base station 30. The received data is processed by the receive circuitry 34 of the base station's modem 28. The processed data is further processed by the modem interface 34 to be in a format suitable for transmission through the RDU 24 and local exchange 22. The data is subsequently transferred through the RDU 24 and local exchange 22 to the user terminal 20.

In the past, wireless communication networks were used primarily to transfer voice signals. However, the demand for wireless transmission of data is ever increasing. In particular, the demand for transmitting high data rates, such as those required for integrated services digital networks (ISDNs), over wireless networks is ever increasing. Accordingly, it is desirable to have a modem interface capable of handling high data rates.

## SUMMARY

A modem interface transfers data between the high data rate interface and a wireless interface. The wireless interface has a plurality of parallel data highways. Each data highway has frames with time slots for transferring data. The plurality of highways outputs data to the high data rate interface and the wireless interface in selected time slots. At least one of the data highways has an input configured to receive data from the high data rate interface in selected time slots. At least one of the data highways has an input configured to receive data from the wireless interface in selected time slots. A processor controls the transfer of data between the plurality of highways.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a wireless communication network.

Figure 2 is a modem interface.

Figure 3 illustrates a wireless communication network carrying integrated services  
5 digital network (ISDN) signals.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 2 illustrates a modem interface 56. As shown in Figure 3, the modem interface  
56 is used to transfer data between a high data rate terminal, such as an integrated services  
digital network (ISDN) terminal 60, and a wireless air interface 38. The modem interface  
56 may be located on the RNT side of the wireless air interface as being a component of the  
RNT 40. Similarly the modem interface 56 may be used on the base station side of the air  
interface 56, such as within the RCS 26. The modem interface 56 is preferably located at  
both the RNT 40 and RCS 26.

If used on the RNT side, the modem interface 56 receives data from the ISDN  
terminal 60 over an ISDN oriented modular-2 highway (IOM-2 highway) 62. Conversely,  
the modem interface 56 also sends data to the ISDN terminal 60 over the IOM-2 highway  
62. If used on the base station side, the modem interface 56 transfers data over a pulse code  
modulation (PCM) highway 62, preferably at an E1 data rate.

Data transmitted to and from the ISDN terminal 60 is sent over eight (8) channels,  
each in a 2B + D format. Data is sent over each of two (2) B channels. Each B channel has  
a data rate of 64 kilobits per second (Kbs). Data is also sent over a D channel having a data  
rate of 16 Kbs. The data sent over the D channel is control data, and is high-level data link  
controlling (HDLC) encoded. Additionally, each channel has a control information (CI)  
channel, an MR channel and an MX channel. The CI channel carries line information at a

## I-2-116.1US

32 Kbs data rate. The MR and MX channels are used for handshake for the CI channel. Each has a data rate of 8 Kbs.

HDLC encoding converts data into frames. Each frame has six (6) fields. Two of these fields are flag fields which are used for synchronization. They indicate the start and end of a frame. An address field identifies the destination for that frame. A control field identifies the function and purpose of the frame. A data field contains the data for transmission. A circular redundancy code (CRC) field is used for error detection and correction.

A PCM/IOM interface 64 transfers data between the IOM-2 or PCM highway 62 and the external PCM highway 66. Preferably, the external PCM highway 66 has a data rate of 2 megabits per second. If used on the RNT side, the PCM/IOM interface 64 converts the PCM data into IOM-2 data and vice versa. If used on the base station side, the PCM/IOM interface 64 merely passes through the PCM data in both directions.

To transfer data between the various components of the modem interface 56, a multiple data highway structure is used, such as three (3) PCM highways I-III 68<sub>1</sub>-68<sub>3</sub> shown in Figure 2. Each PCM highway 68<sub>1</sub>-68<sub>3</sub> uses repeating frames having multiple time slots. A preferred frame would have sixteen (16) time slots numbered from zero to fifteen (TS0-TS15). Each preferred time slot is sixteen (16) bits in length. Each PCM highway 68<sub>1</sub>-68<sub>3</sub> has an associated maximum data rate, such as 2 megabits per second. For three PCM highways 68<sub>1</sub>-68<sub>3</sub>, each having a 2 megabit per second data rate, the combined data rate is 6 megabits per second. Accordingly, multiple PCM highways 68<sub>1</sub>-68<sub>3</sub> with lower data rates, such as 2 megabits per second, can be used to effectively transfer data at a much higher data rate, such as 4, 6 or 8 megabits per second. The multiple PCM highways 68<sub>1</sub>-68<sub>3</sub> allow the modem interface 56 to utilize PCM highways 68<sub>1</sub>-68<sub>3</sub> with a standard data rate, such as 2 megabits per second, and effectively transfer data at a much higher rate. Using a standard

data rate PCM highway  $68_1-68_3$  simplifies the structure of the highways  $68_1-68_3$ . Additionally, since the multiple highways  $68_1-68_3$  can be selected to have the same data rate as the PCM highway 66, only a single clock domain is required for the highways 66,  $68_1-68_3$ . As a result, power consumption and noise are reduced and testability is improved.

5 Clock routing is also simplified by using only a single clock domain.

One possible assignment using three (3) PCM highways  $68_1-68_3$ , each having 16 time slots (TS0-TS15) is as follows. For PCM highway I  $68_1$ , TS0-TS15 are all assigned to transferring data to and from the external PCM highway 66 and the PCM highway I  $68_1$ . A group of read devices  $70_1-70_n$  read data from the corresponding time slots on PCM highway I  $68_1$  and a corresponding group of write devices  $72_1-72_n$  write that read data onto the IOM PCM highway 66. Conversely, a group of read devices  $74_1-74_n$  read data from the IOM PCM highway 66 and a corresponding group of write devices  $76_1-76_n$  write that data onto the corresponding slots on PCM highway I  $68_1$ .

Each write device is fixed to a predetermined time slot. Each read device can read data from any time slot on any highway  $68_1-68_3$ . The advanced instruction set computer (ARM) processor 88 controls which time slot that each read device reads.

The external PCM highway 66 preferably uses repeating frames of 125 microsecond duration. The read devices  $74_1-74_n$  can read data starting at any bit in the frame and at a variety of data rates. The starting bit is controlled by a PCM slot parameter and the data rate is controlled by a PCM rate parameter. The ARM processor 88 determines the PCM slot and rate parameters.

PCM highway II  $68_2$  is used to transfer data to and from the digital signal processor (DSP) 78 using TS0-TS7. One such DSP 78 is a 54x family processor, preferably a TMS320C54x processor. The DSP 78 may perform functions such as speech, video compression or encryption. Data is read from the PCM highway II  $68_2$  using a group of read

devices 80<sub>1</sub>-80<sub>n</sub>. The read data is buffered by a group of buffers 84<sub>1</sub>-84<sub>n</sub> and then sent to the DSP 78. Data sent from the DSP 78 is buffered by a group of buffers 86<sub>1</sub> and then written into the corresponding time slots of the PCM highway II 68<sub>2</sub> using a group of write devices 82<sub>1</sub>-82<sub>n</sub>. TS8 - TS15 of the PCM highway II 68<sub>2</sub> are used to interface with telephone interface components.

The ARM processor 88 typically has an associated external flash memory. The ARM processor 88 controls various aspects of the modem 48. Data is read from TS8-TS15 using a group of read devices 90<sub>1</sub>-90<sub>n</sub>. The read data is buffered by a group of buffers 92<sub>1</sub>-92<sub>n</sub> and sent to an IOM interrupt device 98 and the ARM processor 88. The output from the IOM interrupt device 98 is also input to the ARM processor 88. The IOM interrupt device 98 determines whether the C/I channel data has changed from frame to frame and will notify the ARM processor 88 when a change is detected. Conversely, the ARM processor 88 sends data to a group of buffers 94<sub>1</sub>-94<sub>n</sub>. Write devices 96<sub>1</sub>-96<sub>n</sub> take the buffered data and write it to the corresponding time slots of the PCM highway II 68<sub>2</sub>.

An ARM port interface (API) 140 is a shared memory interface between the ARM processor 88 and the DSP 78 and transfers control signals between the ARM 88 and DSP 78. The API 140 preferably has a two kiloword block of memory. The DSP 78 is slaved to the ARM 88. The ARM 88 controls the interrupts and resets of the DSP 78. Conversely, the DSP 78 can interrupt the ARM processor 88.

TS0-TS8 of PCM highway III 68<sub>3</sub> are used for HDLC processing. Data in TS0-TS8 are read by the HDLC reading devices 108<sub>1</sub>-108<sub>n</sub>. Data from TS0 - TS2 is processed by an HDLC multiplexer (HMUX) 112 which sends processed data to an input/output (I/O) device 116 and an HDLC I controller 114<sub>1</sub>. Data is also sent from the I/O devices 116 and HDLC I controller 114<sub>1</sub> to the HMUX 112. The data processed by the HMUX 112 from the I/O device 116 and HDLC I device 114<sub>1</sub> is written to TS0-TS2 of PCM highway III 68<sub>3</sub> using

a HDLC write device 110<sub>1</sub>. Data in TS3-TS8 is transferred to and from the other two HDLC controllers (HDLC II 110<sub>2</sub>, TS3-TS5, and HDLC III 110<sub>3</sub>, TS6-TS8). The data in the corresponding slots is read by HDLC read devices 108<sub>2</sub>, 108<sub>3</sub> prior to being sent to the corresponding HDLC controller 114<sub>2</sub>, 114<sub>3</sub>. Data from the HDLC II 114<sub>2</sub> and HDLC III 114<sub>3</sub> controllers is sent to the HDLC write devices 110<sub>2</sub>, 110<sub>3</sub> and written onto the corresponding slots of PCM highway III 68<sub>3</sub>. Data from each of the three HDLC controllers (HDLC I 114<sub>1</sub>, HDLC II 114<sub>2</sub> and HDLC III 114<sub>3</sub>) is transferred back and forth to the ARM processor 88. The HDLC controllers 114<sub>1</sub>-114<sub>3</sub> are used to communicate with the ARM processor 88 or the traffic channels.

The HDLC controllers (HDLC I 114<sub>1</sub>, HDLC II 114<sub>2</sub> and HDLC III 114<sub>3</sub>) are used to encode the D channel for transfer over the air interface 38 and decode the D channel after transmission over the air interface 38. As previously mentioned, the D channel is HDLC encoded. To assure that the integrity of the HDLC encoding is preserved after transmission over the air interface 38, the D channel is again HDLC encoded prior to transmission across the wireless air interface 38 by the HDLC controllers 114<sub>1</sub>-114<sub>3</sub>. Accordingly, the control data is double HDLC encoded. This double encoding allows for error correction over the air interface 38 and for the integrity of the originally HDLC encoded D channel to be maintained.

Conversely, the HDLC controllers 114<sub>1</sub>-114<sub>3</sub> also decode a double HDLC encoded D channel received over the wireless interface 38. The double HDLC encoded D channel is stripped of the second HDLC encoding by the HDLC controllers 114<sub>1</sub>-114<sub>3</sub>. The CRC field data is used to correct any errors that occurred during the wireless transfer. Accordingly, the original D channel is recovered. Preferably, each HDLC controller 114<sub>1</sub>-114<sub>3</sub> processes data at 384 Kbs and require 3 128 Kbs time slots.

TS9-11 of PCM highway III 68<sub>3</sub> are used to transfer data to and from the ARM

processor 88. A group of read devices  $100_1-100_n$  read data from the corresponding slots of PCM highway III  $68_3$ . The read data is buffered by a group of buffers  $102_1-102_n$  and is sent to the ARM processor 88. The ARM processor 88 sends data to a group of buffers  $94_1-94_n$ . The buffered data is written by corresponding write devices onto PCM highway III  $68_3$ .

5           If the modem interface 56 is used at a base station, the frame synchronization and clock are input to the interface 56. If used in a RNT 40, the frame synchronization and clock are generated by the RNT 40, such as on an application specific integrated circuit (ASIC) containing the interface 56.

TS12-TS15 of PCM highway III  $68_3$  are used to carry data received over the air interface 38 and to be sent over the air interface 38. Data received over the air interface 38 is preferably modulated using quadrature phase shift keying (QPSK), although other modulation schemes may be used. Prior to being input to the modem interface 56, the received data is decoded using a double speed quadrature viterbi decoder, although other decoding schemes may be used. The viterbi decoder preferably decodes four received traffic channels (QVD\_TR0 - QVD\_TR3). Preferably, the data rates supported are 8, 16, 32, 64, 128 Kbs. The ARM processor 88 controls the read assignments to the multiple PCM highways  $68_1-68_3$  effectively controlling data routing and data rate.

20           Data to be sent over the air interface 38 is preferably convolutionally encoded, spread and transmitted using QPSK modulation, although other wireless transmission schemes may be used. The data is preferably sent over four traffic channels (TR0-TR3).

25           Data to be sent over the wireless interface 38 is read by a group of read devices  $118_1-118_4$ . One read device  $118_1-118_4$  is used per traffic channel, TR0-TR3. Another set of read devices is used for encryption of each channels data  $120_1-120_4$ . The output of one  $120_1-120_4$  of each channel's encryption read devices is input into a parallel to serial converter  $122_1-122_4$ . The serial output of that converter  $124_1-124_4$  is fed into another parallel to serial

converter  $124_1-124_4$  which also receives the output of the other one of that channel's read devices  $118_1-118_4$ . The two serial outputs are modulo-2 added on a bit basis to encrypt the data. Each channel's encrypted serial output is typically sent to a corresponding convolutional encoder, spreader and modulator for transfer over the wireless interface 38.

- 5 Each parallel to serial converter  $118_1-118_4$  is programmed to produce data at a desired bit rate.

Encrypted data received from traffic channels, such as QVD\_TR0-QVD\_TR3, is input to a group of serial to parallel converters  $126_1-126_4$ . Each channel's serial to parallel converter  $126_1-126_4$  combines that traffic channel's data with an output of a parallel to serial converter  $128_1-128_4$  to decrypt the traffic data. The decryption data from each parallel to serial converter  $128_1-128_4$  originates from data read from TS12-TS15 by corresponding read devices  $138_1-138_4$ . The read data is converted from parallel to serial format by the parallel to serial converters  $128_1-128_4$ . The serial outputs of the serial to parallel converters  $126_1-126_4$  are inputted to a group of write devices  $132_1-132_4$  which write the serial output to a group of multiplexers  $130_1-130_4$ . The multiplexed data is sent to TS12-TS15 of the PCM highway III 68<sub>3</sub>. For testing, the DSP 78 outputs a signal to a group of buffers  $136_1-136_4$ . The output of the buffers  $136_1-136_4$  is also input to the multiplexers  $130_1-130_4$ .

\*

\*

\*

CLAIMS

What is claimed is:

1. A modem interface for transferring data between a high data rate interface and a wireless interface, the modem interface comprising:

a plurality of parallel data highways having frames with time slots for transferring data, the plurality of data highways outputting data to the high data rate interface and the wireless interface in selected time slots;

at least one of the data highways having an input configured to receive data from the high data rate interface in selected time slots;

at least one of the data highways having an input configured to receive data from the wireless interface in selected time slots; and

a processor for controlling data transfer between the plurality of data highways.

2. The modem interface of claim 1 wherein the high data rate interface is an IOM-2 highway.

3. The modem interface of claim 1 wherein the high data rate interface is a PCM highway.

4. The modem interface of claim 1 wherein the plurality of parallel data highways is three parallel data highways.

5. The modem interface of claim 4 wherein each of the three parallel data highways has a 2 Mbs data rate.

6. The modem interface of claim 1 further comprising a plurality of read and write devices, each write device fixedly writes to one of the plurality of data highways and each read device is capable of reading data from any of the plurality of data highways.

7. The modem interface of claim 6 wherein the processor controls each read device so that that read device reads from a selected one of the data highways.

8. The modem interface of claim 1 wherein the frames have sixteen time slots.

9. A method for transferring data between a high data rate interface and a wireless interface, the method comprising:

providing a plurality of parallel data highways having frames with time slots for transferring data;

inputting data to the data highways from the high data rate interface and the wireless interface in selected time slots;

controlling data transfer between the plurality of highways; and

outputting data to the high data rate interface and the wireless interface in selected time slots.

10. The method of claim 9 wherein the high data rate interface is an IOM-2 highway.

11. The method of claim 9 wherein the high data rate interface is a PCM highway.

12. The method of claim 9 wherein the plurality of parallel data highways is three parallel data highways.

13. The method of claim 9 wherein each of the three parallel data highways has a 2 Mbs data rate.

14. The method of claim 9 wherein the data transfer is controlled using a plurality of read and write devices, each write device fixedly writes to one of the plurality of data highways and each read device is capable of reading data from any of the plurality of data highways.

15. A radio network terminal (RNT) transferring data between a high data rate interface and a wireless interface, the RNT comprising:

a receiver and a transmitter for transferring data over the wireless interface;

an input and output for transferring data over the high data rate interface;

5 a plurality of parallel data highways having frames with time slots for transferring data, the plurality of data highways outputting data to the high data rate interface and the wireless interface in selected time slots;

at least one of the data highways having an input configured to receive data from the high data rate interface in selected time slots;

10 at least one of the data highways having an input configured to receive data from the wireless interface in selected time slots; and

a processor for controlling data transfer between the plurality of highways.

16. The RNT of claim 15 wherein the receiver and transmitter transfer data using QPSK modulation in CDMA format.

17. The RNT of claim 15 wherein the RNT is operatively couple to an ISDN terminal via the high data rate interface.

18. The RNT of claim 15 wherein the frames have sixteen time slots.

19. The RNT of claim 15 wherein the plurality of parallel data highways is three parallel data highways.

20. The RNT of claim 15 wherein the high data rate highway is an IOM-2 highway.

21. A method of communicating data over a wireless interface of a wireless communication network having a first and second communication station, the method comprising:

producing data having a first high-level data link controlling (HDLC) encoding at the first station for transfer over the wireless interface;

encoding the first HDLC encoded data into a second HDLC format such that the produced data is double HDLC encoded;

transmitting the double HDLC encoded data over the wireless interface;

receiving the double HDLC encoded data at the second station; and

removing the second HDLC encoding to recover the first HDLC encoded data at the second station.

I-2-116.1US

22. The method of claim 21 wherein the first station is a RNT and the second station is a RCS, further comprising:

prior to producing the first HDLC encoded data, receiving the first HDLC encoded data from an IOM-2 highway.

23. The method of claim 21 wherein the first station is a RCS and the second station is a RNT, further comprising:

prior to producing the first HDLC encoded data, receiving the first HDLC encoded data from a PCM highway.

## ABSTRACT

A modem interface transfers data between the high data rate interface and a wireless interface. The wireless interface has a plurality of parallel data highways. Each data highway has frames with time slots for transferring data. The plurality of highways outputs data to the high data rate interface and the wireless interface in selected time slots. At least one of the data highways has an input configured to receive data from the high data rate interface in selected time slots. At least one of the data highways has an input configured to receive data from the wireless interface in selected time slots. A processor controls the transfer of data between the plurality of highways.

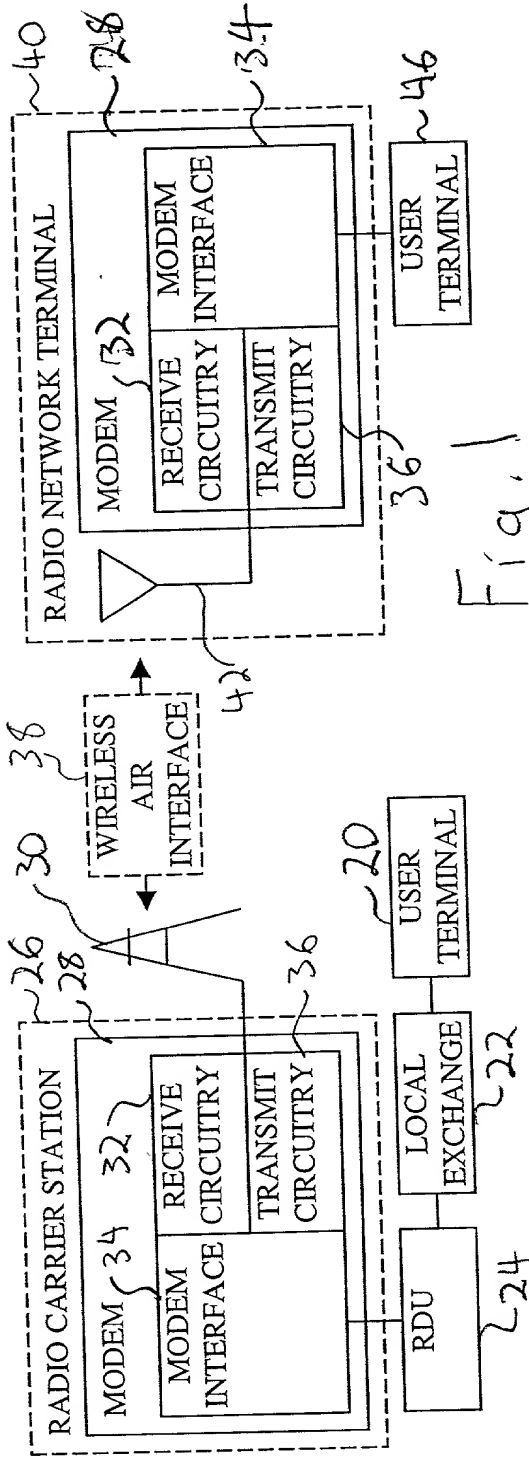


Fig. 1

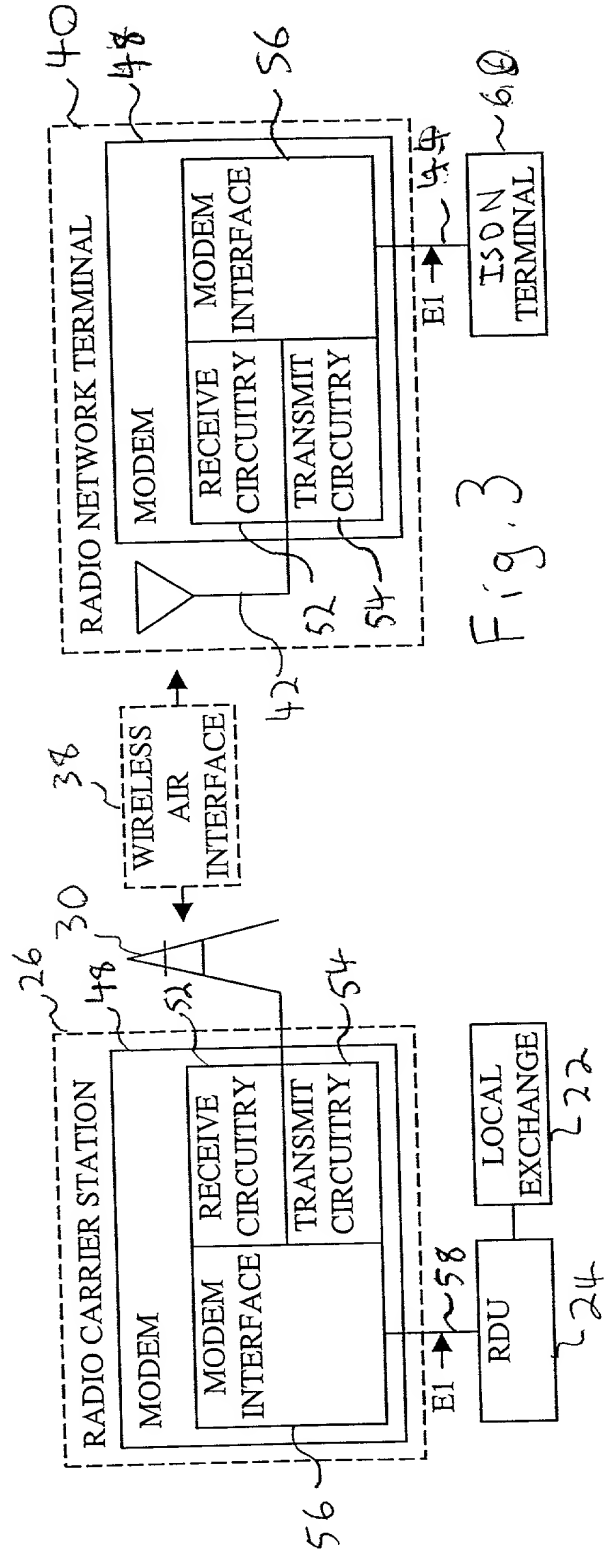


Fig. 3

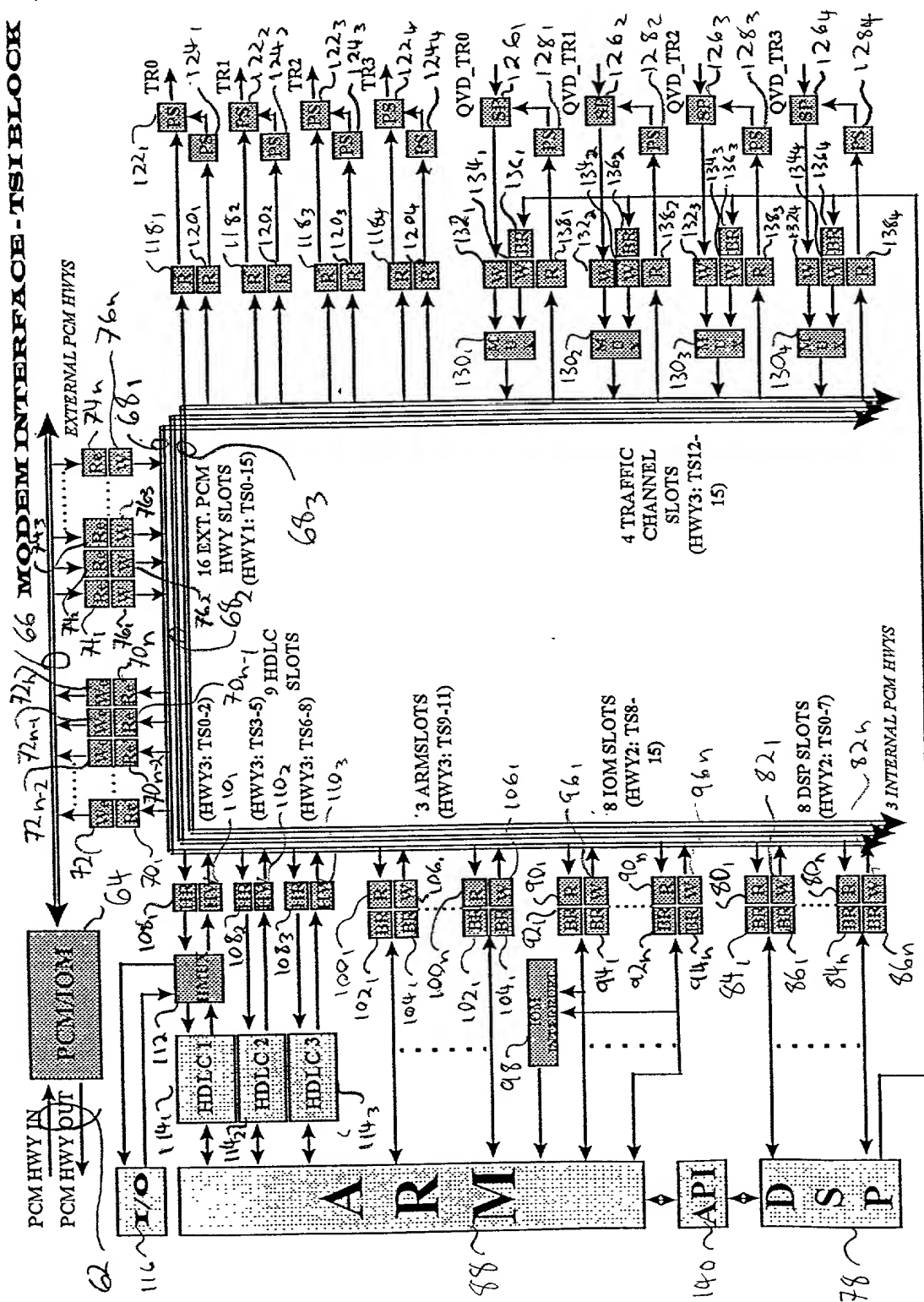


Fig. 2

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	<b>First Named Inventor</b>	Kaewell, Jr. et al.
	<b>COMPLETE IF KNOWN</b>	
	Application Number	Not Yet Known
	Filing Date	Not Yet Known
	Group Art Unit	Not Yet Known
	Examiner Name	Not Yet Known

**As a below named inventor, I hereby declare that:**

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

**MODEM INTERFACE**

the specification of which (Title of the Invention)

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OR  
☐ was filed on (MM/DD/YYYY) as United States Application Number or PCT International Application Number and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above

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Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
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			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

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Application Number(s)	Filing Date (MM/DD/YYYY)	<input type="checkbox"/> Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.
60/192,230	03/27/2000	

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Name of Sole or First Inventor:

☐ A petition has been filed for this unsigned inventor

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☒ Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

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## DECLARATION

ADDITIONAL INVENTOR(S)  
Supplemental Sheet  
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<b>Name of Additional Joint Inventor, if any:</b>				<input type="checkbox"/> A petition has been filed for this unsigned inventor			
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Post Office Address							
City		Bellmore	State	NY	ZIP	11710	Country
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<b>Name of Additional Joint Inventor, if any:</b>				<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name (first and middle [if any])				Family Name or Surname			
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Residence: City			State		Country		Citizenship
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